A More Accurate Current-Mode Control Model

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Abstract

For working power supply engineers, the Unitrode handbook is often the standard reference for control analysis. This paper gives a very simple extension to the existing Unitrode models that accounts for the subharmonic oscillation phenomenon seen in current-mode controlled converters. Without needing any complex analysis, the oscillation phenomenon, ramp addition, and control transfer function are unified in a single model.

I. Introduction

This paper provides the simple results needed to augment the existing single-pole model typically used for current-mode control. These results will allow you to:

1. Model and predict control transfer functions with greater accuracy.
2. Select the proper compensation ramp.
3. Use a single small-signal model for both transfer functions and current loop stabilization.
4. Decide when you need to add a ramp to your power circuit, and how much to add.

The analytical results presented here are the result of complex modeling techniques using sampled-data. Once armed with these equations understanding and designing your current loop becomes very simple. You don't need to be familiar with any of the more complex analysis techniques to get the full benefits of the extended model.

All of the analysis results presented here are incorporated in the Power 4-5-6 design software. This software makes it easy for you to use the latest and most accurate models for your power converter design and control.

Methods of implementing the compensating ramp in your circuit are also discussed. The usual methods suggested by the control IC manufacturers are not recommended for rugged and predictable operation.

II. Basic Current-Source Dynamics

The basic concept of current mode control is shown in Fig. 1.

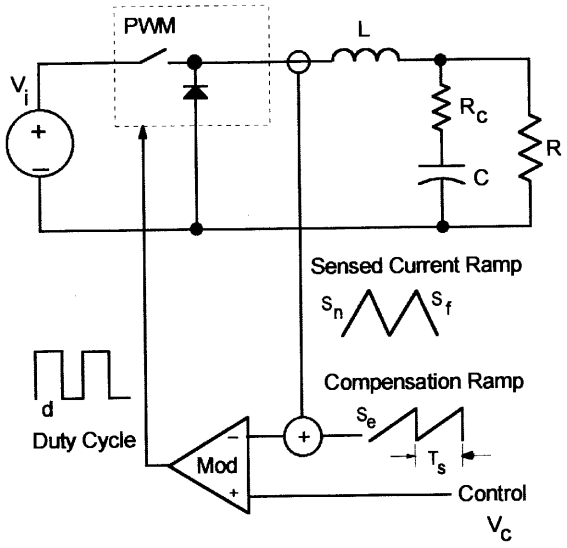

Fig. 1 – Peak current-mode control circuit.

Instead of using just a sawtooth ramp to control the duty cycle of the converter, a signal proportional to the inductor current is summed with a sawtooth ramp. In some

cases, the sawtooth ramp is omitted completely, and the error voltage signal, V_c, controls the peak value of the inductor current.

We don't usually sense the inductor current directly – it's often inconvenient or inefficient to do this. Usually, the power switch current is sensed to gather the information about the inductor current.

Early analyses of this control assumed ideal control of the current, and modeled the system by viewing the inductor as a controlled current source. This is the basis of the widely used models presented in an early paper [1] and Unitrode handbooks [2].

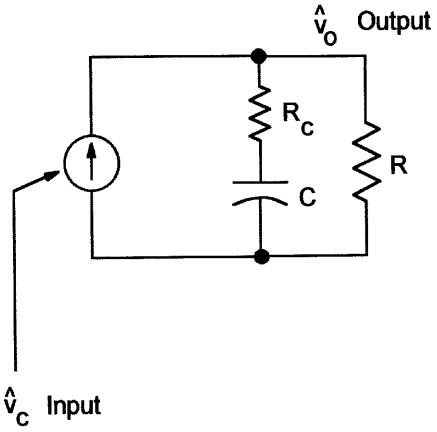

Fig. 2: Simplest small-signal model – current source feeding the load.

III. Subharmonic Oscillation

The current-source analogy works fine under many conditions, but with one problem: the system can oscillate! This is of course, well known and documented. And, we all know retaining the sawtooth compensating ramp in the control system eliminates the problem – but most small-signal models don't tell you what this does to the control characteristics.

Fig. 3: shows the nature of the current loop oscillation. At duty cycles approaching 50% and beyond, the peak current is regulated at a fixed value, but the current will oscillate back and forth on subsequent switching cycles.

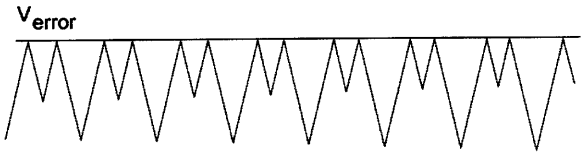

Fig. 3: Subharmonic oscillation waveforms.

The situation is really very simple, as pointed out by Holland [3] in an early paper – the current-mode oscillation is like any other oscillation – if it's undamped, it will continue to ring, and grow in amplitude under some conditions. If it's damped, the oscillations decrease and die out.

The sampled-data or discrete-time analysis of this phenomenon, required because of its high frequency, has been with us for some time. So why don't most engineers use this in their work? Because the analysis is usually too complex. However, it has been shown [4] that very practical results can be simplified into an easily usable form.

IV. Sampled-Data Analysis

Early modeling combined simple average analysis with separate explanations of how the current signal could become unstable. However, the small-signal model and physical explanation for instability were never reconciled until [4]. This paper expanded upon earlier work [5], but found a way to simplify the results into a more useful format.

Other analyses have subsequently analyzed the same issue. Many of these agree in the way the problem is tackled and provide supporting experimental data. Others disagree in the methods but still come to the same conclusions about the second-order oscillatory system that results. They are all consistent in the values derived.

That's good news – we don't need to get hung up in conflicting sampled-data modeling techniques, or debates about how to analyze a system, we can use the common design equations everyone agrees on, and get on with the job of getting product out of the door.

V. Dominant Pole Models

The equivalent control system diagram for current mode control is shown in Fig. 4. The inductor current feedback becomes an inner feedback loop. We are usually concerned with the transfer function from the control input shown to the output of the power converter. The input is typically the input to the duty cycle modulator, provided by the error amplifier output.

Most designers are familiar with the fact that the current feedback loop reduces the main dynamic of the system to a dominant single-pole type response. This is a result of viewing the inductor as a controlled current source rather than as a state of the system.

The results of existing analysis for the three main types of converter are summarized below.

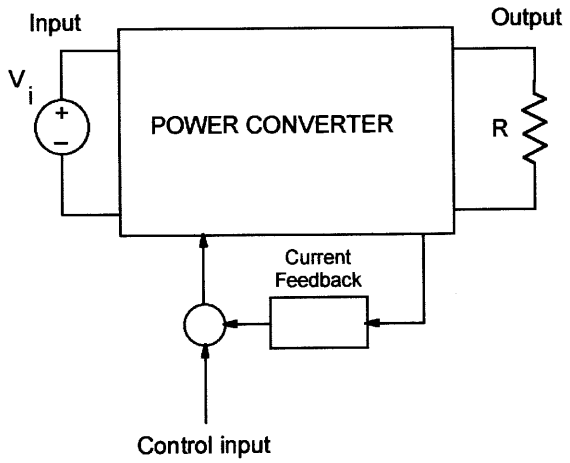

Fig. 4: Control system representation of current-mode control. Current loop is embedded in the system.

A. Buck Converter

The low-frequency model of the buck converter, commonly used by designers, and summarized in [2] is given by:

$$f_p(s) = K\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}}$$

The load resistor and capacitor determine the dominant pole, as we would expect for a current source feeding an RC network, shown in Fig. 3.

$$\omega_p = \frac{1}{RC}$$

In [4] there is a more accurate expression for the dominant pole of the buck, involving the external ramp and operating point of the converter:

$$\omega_p = \frac{1}{RC} + \frac{T_s}{LC}(m_c D' - 0.5)$$

However, this refinement is usually unnecessary. It only becomes important when too steep a ramp is used, showing how the pole can move. In most cases, the simplified form of the dominant pole is adequate for design purposes.

The power stage transfer function zero is determined by the equivalent series resistance of the capacitor:

$$\omega_z = \frac{1}{R_c C}$$

This expression for the output capacitor zero is the same for all the converters.

B. Boost Converter

The boost converter has an additional term in the control transfer function, caused by the right-half-plane (rhp) zero of the converter:

$$f_p(s) = K\frac{\left[1+\frac{s}{\omega_z}\right]\left[1-\frac{s}{\omega_{z\,rhp}}\right]}{1+\frac{s}{\omega_p}}$$

The dominant pole is located at

$$\omega_p = \frac{2}{RC}$$

and the rhp zero is at

$$\omega_{z\,rhp} = \frac{R(1-D)^2}{L}$$

Note that the rhp zero expression is exactly the same as that for voltage mode control. Using current mode does not move this at all, although it is easier to compensate for since we do not also have to deal with the double pole response of the LC filter that is present with voltage mode control.

C. Flyback Converter

The flyback converter also has a rhp zero term in the control transfer function:

$$f_p(s) = K \frac{\left[1+\frac{s}{\omega_z}\right]\left[1-\frac{s}{\omega_{z\,rhp}}\right]}{1+\frac{s}{\omega_p}}$$

with the dominant pole determined by

$$\omega_p = \frac{1+D}{RC}$$

and the rhp zero at:

$$\omega_{z\,rhp} = \frac{R(1-D)^2}{DL}$$

As with the boost converter, this zero location is the same as for voltage mode control.

VI. Measured High-Frequency Effects

To account for the observed oscillation in the current mode system, we need to add a high-frequency correction term to the basic power stage transfer functions.

The converter transfer functions are modified from the above section by

$$f_p'(s) = f_p(s) f_h(s)$$

Without even considering the sampled-data type analysis, we can see what the form of the transfer function has to be. One way it becomes clear is to measure the control-to-output transfer functions, while adding different amounts of compensating ramp to the system.

Fig. 5 shows measurements of power stage transfer functions plotted beyond half the switching frequency. The characteristic at half the switching frequency is a classic double pole response that can be seen in any fundamental text on bode plots and control theory.

These curves are for a buck converter operating at a 45% duty cycle. In the upper curve, there is no compensating ramp added, and there is a sharp peak in the transfer function at half the switching frequency.

The curves below this have increasing amounts of compensating ramp added to them, until the bottom curve is reached and the double poles are overdamped.

Once you make this series of measurements, the need for the correction to the power stage transfer function becomes obvious.

Mathematical theoreticians may argue that measuring and predicting transfer functions up to this frequency is of questionable analytical merit. However, there is such a direct correlation between the measurements and the oscillatory behavior of the system, that the correction term is vital for good and practical modeling.

When the system transfer function peaks with a high Q, the inductor current oscillates back and forth, as shown in Fig. 6. When the transfer function is well damped, the inductor current behaves, returning quickly to equilibrium after an initial disturbance.

Including this high frequency extension in the model is a very practical and powerful tool – it has real meaning to the designer.

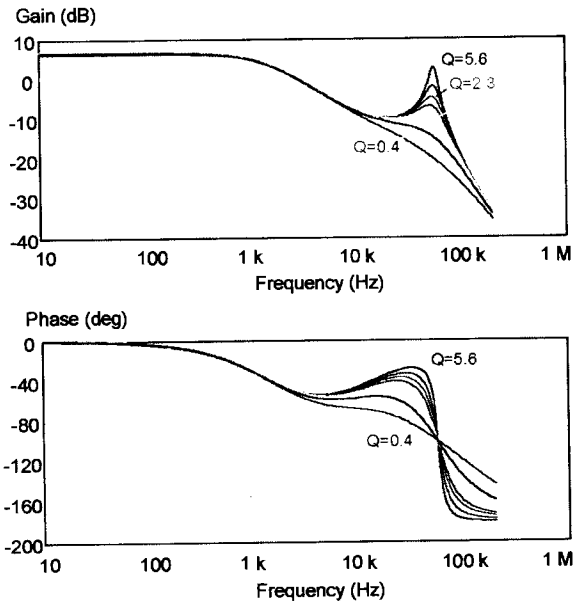

Fig. 5: Power stage transfer functions plotted up to the switching frequency. Notice the obvious double-pole characteristic centered at half the switching frequency.

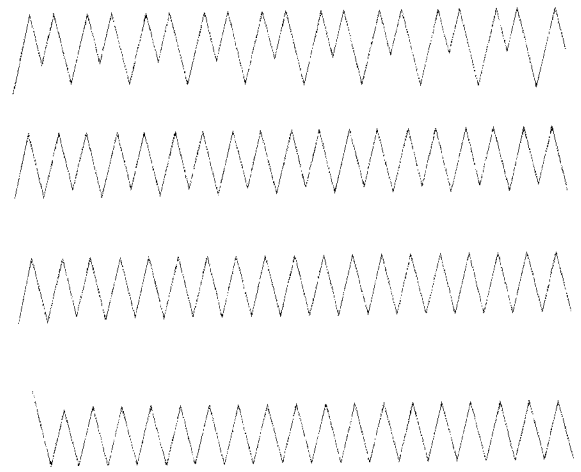

Fig. 6: Inductor current oscillation waveforms. Waveforms correspond to a Q of 7.6, 5.6, 2.3 and 0.7.

VII. Analytical Results

The qualitative understanding of the double poles is obvious. Quantitative analysis via sampled-data, or other methods gives the simple transfer function parameters to be used for design.

The high frequency term is a common expression for all given by

$$f_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}}$$

where the double-pole oscillation is at half the switching frequency.

$$\omega_n = \frac{\pi}{T_s}$$

The damping is given by

$$Q_p = \frac{1}{\pi(m_c D' - 0.5)}$$

The compensation ramp factor is given by

$$m_c = 1 + \frac{s_e}{s_n}$$

where the compensating ramp slope, se, is

$$s_e = \frac{V_{p-p}}{T_s}$$

and the slope of the sensed current waveform into the PWM controller is

$$s_n = \frac{V_{on}}{L} R_i$$

R_i is the gain from the inductor current to the sensed voltage fed into the control PWM, and V_{on} is the voltage across the inductor when the switch is on. For a simple nonisolated converter with resistive sensing, R_i is the value of the sense resistor.

These equations are useful for anyone wanting to model their converter and predict its response. They will give much more accurate results than simple single-pole models.

For those not interested in modeling, who don't have time and just need to get on with building a converter, the equations give you

the information you need for design, as explained in the next section.

VIII. How Much Ramp?

So what do you need to do with this information? The answer is simple – make sure your current loop won't oscillate. Or, in small-signal analysis terms, make sure the Q of the double pole is one or less. And how do you do this? Just by adding a compensating ramp, as all previous papers advise.

How much ramp do you add? Well, going by the small-signal theory, we just set the Q of the double poles to one, and solve the resulting system. Most early publications express the amount of ramp added in terms of the off-time ramp slope, S_f. If we solve the equation for Q_p in the same terms, the result is:

$$\frac{s_e}{s_f} = 1 - \frac{0.18}{D}$$

This is not quite the same as other suggestions. Some publications recommend adding as much ramp as the downslope. This is more than is needed, overdamping the system.

Others suggest adding half as much ramp as the downslope of the inductor current. For the buck converter, in theory, this cancels all perturbations from input to output. In practice, this nulling is never achieved completely, a small amount of noise makes it impossible.

Another question is when should you start adding a ramp to a system? Earlier simplistic analysis says that no ramp is needed until you reach a 50% duty cycle. There is something troubling about this. A power supply is an analog circuit. It would be a little strange if it were fine at 49.9% duty cycle, and unstable at 50.1%. The analog world just does not behave that way. In the real world, you often need to start adding a compensation ramp well before a 50% duty cycle is reached.

The design equation above continues to add ramp down to an 18% duty cycle in order to keep the Q_p of the current-mode double pole equal to 1. This is probably overly conservative – a more practical value for starting to add a compensating ramp is at D=36%.

IX. Instability at Less Than 50% Duty

Many publications, especially those from the manufacturers of control chips, explicitly tell you that you don't need to use a compensating ramp in the circuit at duty cycles less than 50%. This conflicts with the suggestions given above.

So what should you do? There are some special circuit conditions that cause this seeming contradiction in analysis results.

First, remember that the current loop oscillation is *only* a problem with continuous conduction operation (CCM) near or above 50% duty cycle. Many converters are operated in discontinuous conduction mode (DCM), especially flyback converters that are the most popular choice for low power outputs.

Secondly, if you choose to use a control chip such as the UC1842, this chip has a *maximum* duty cycle capability of just under 50%. That does not mean that the converter will ever operate in that region – typically it will never see more than perhaps a 40% duty cycle. More often than not, this will not be a severe problem.

But sometimes, with low input line, you will operate a converter close to 50%, and you may need to add ramp to compensate the current loop. Consider a case of a 44% duty cycle. The double pole peaking is determined by

$$Q_p = \frac{1}{\pi(0.56 - 0.5)} = 5.6$$

This can get you into trouble. Look at the power stage gain (lower curve) in Fig. 7. The peaking on this curve corresponds to a Q_p of

5.6. With just the current feedback loop closed, the system is stable – the current will bounce back and forth, but the oscillations eventually die down, as shown in Fig. 8.

Now consider what happens when the voltage regulation loop is closed. With a crossover frequency of 14 kHz (reasonable for a 110 kHz converter), the phase margin at this initial crossover frequency is close to 90 degrees.

But the loop gain crosses over the 0 dB axis *again* just before half the switching frequency, this time with no phase margin at all. The waveforms of Fig. 9 are the result – severe oscillation in the current loop.

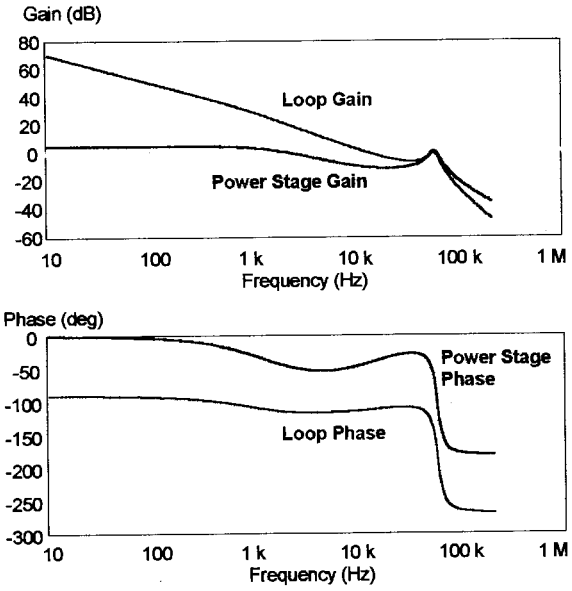

Figure 7: Current mode instability at less than 50% duty cycle. Adding compensation to the power stage transfer function causes the resulting loop gain to peak up and crossover again at half the switching frequency.

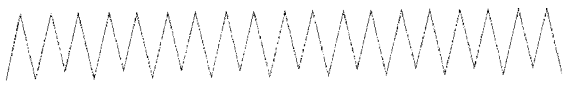

Figure 8: Inductor current waveforms at D=0.44 with only the current loop closed.

Figure 9: Inductor current waveforms at D=0.44, with outer feedback loop closed. System is now unstable, as shown by the loop gain of Fig. 7. A plot without the double pole extension to the model does not predict this oscillation.

This example clearly shows why the high-frequency extension is needed to the model. Without it, the current loop oscillation at less than 50% duty cycle cannot be predicted.

X. Magnetizing Ramp Addition

Some readers of this may say – "I've built converters at 45% duty cycle before and never had any problem – what's the issue here?" And they are quite correct. If you are building any kind of forward converter, or other isolated buck-derived topology, and sensing on the primary switch side, you often get a free ramp.

The magnetizing current of the main power transformer contributes a signal in addition to the reflected output inductor current, and this works in exactly the same way as the compensating ramp. The amount of slope contributed by the magnetizing current is given by

$$s'_e = \frac{V_i}{L_M} R_i$$

You should always check this value when doing your design. In most cases, the amount of ramp that you get due to the magnetizing current is more than enough to damp the double pole properly. In fact, the opposite is frequently true – the amount of ramp can often be excessive, especially for converters with low output ripple current, and the system can be very overdamped. This creates additional phase delay in the control to output

transfer function, as can be seen in Fig. 5 in the lowermost curve.

XI. How to Add the Ramp

A comment on ramp addition from field experience rather than the chip manufacturer's viewpoint is appropriate. This is a topic frequently dismissed as trivial, but it is very important if you want to get the best performance out of your current-mode system.

Ridley Engineering has taught control design courses, both theoretical, and hands- on for many years [6]. In designing current-mode control test circuits for these labs, we observed that the predicted and measured responses do not match well at all with conventional schemes for adding a ramp to a converter.

The simplest proposed method for ramp addition is to resistively sum the clock sawtooth signal with the sensed current signal shown in Fig. 10. This must be done with a high value of resistor in order not to overload the somewhat delicate clock signal. It provides a high-impedance, noise-susceptible signal for use by the control comparator.

It also connects additional components to the clock pin, and will affect the clock waveforms.

The sensitivity of the clock pin cannot be stressed enough. The Unitrode application notes tell you to put the timing capacitor close to the chip, but they do not emphasize this as much as perhaps they should. The timing capacitor is the most crucial component in the control circuit, and it should be placed first during layout, as physically close to the pins of the control chip as can be achieved.

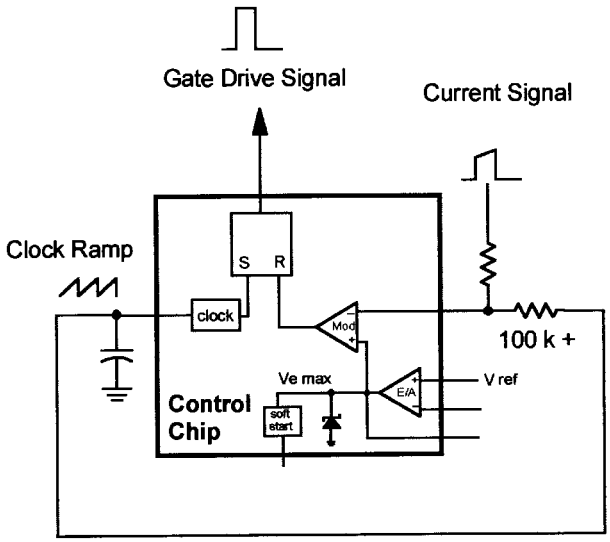

Figure 10: Resistive summing of the timing ramp and current signal for ramp addition. This circuit is NOT recommended. The clock signal is very sensitive to loading and noise, and can lead to power supply failure if it is corrupted.

If you don't do this, the results can be catastrophic. On one low-power off line converter, the timing capacitor was placed ¼" away from the pins, without a ground plane. When the converter was started up, the clock signal picked up switching noise, and briefly ran at 1 MHz instead of the desired 100 kHz. The resulting stress on the power switch was sufficient to cause failure. Moving the capacitor closer to the IC pins cured the problem.

Given this level of sensitivity, it is a good idea not to use the clock signal for *anything* except its intended purpose. Any additional components connected to the timing capacitor introduce the potential for noise into that node of the circuit. Even the buffered clock signal technique, shown in Fig. 11, can cause problems.

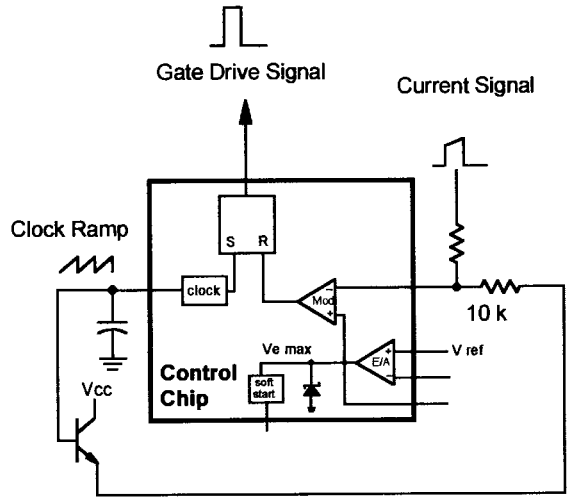

Figure 11: Buffered signal adding the timing ramp and current signal for ramp addition.This allows a lower summing resistor and better noise immunity. However, it is still not recommended to load the clock, even with a transistor.

An alternative approach to generating the ramp signal for current-mode compensation is shown in Fig. 12. This method uses the output drive signal, loaded with an RC network, to generate a compensation ramp to sum with the current mode signal.

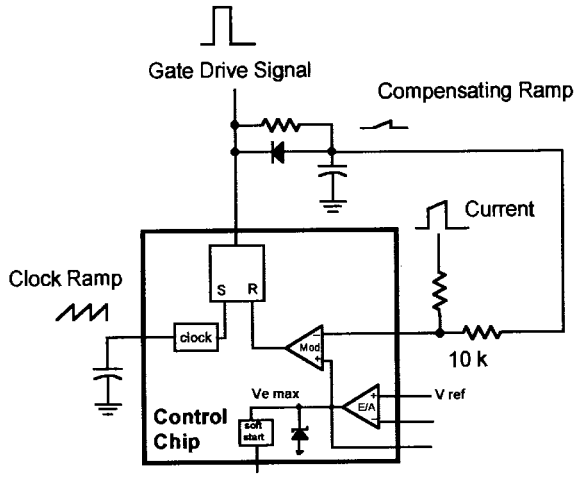

Figure 12: The best way to generate the compensation ramp is independently from the clock signal. The output gate drive signal provides a convenient way to do this.

XII. Conclusions

A simple extension to the common single-pole models can greatly enhance the accuracy and usefulness of current-mode control modeling. This allows you to design your power supply for peak performance.

Simple equations help you to select the proper ramp for compensating the current feedback loop, and to predict the correct control-to-output voltage transfer function. These equations show how a current-mode power supply can sometimes go unstable - even at duty cycles less than 50%.

Correlation between measured transfer functions, up to half the switching frequency, and observed circuit oscillations or jitter are very good.

Actual circuit implementation of the compensating ramp should be done very carefully. The clock signal should *not* be used for this function if you want to design the most rugged and reliable power supply.

Generating a low-noise compensating ramp will also provide a power supply with measurements that closely agree with predictions. This is a crucial factor in many industries, such as aerospace, where the customer expects delivered product and accurate circuit models.

Ray Ridley has specialized in the modeling, design, analysis, and measurement of switching power supplies for over 20 years. He has designed many power converters that have been placed in successful commercial production. In addition he has consulted both on the design of power converters and on the engineering processes required for successful power converter designs.

Ridley Engineering, Inc. is a recognized industry leader in switching power supply design, and is the only company today offering a combination of the most advanced application theory, design software, design hardware, training courses, and in-depth modeling of power systems.

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6. Ridley Engineering, Inc. *"Modeling and Control for Switching Power Supplies"* professional engineering seminar taught semi-annually. See [8].

7. Switching power supply design information, design tips, frequency response analyzers, and educational material for power supplies can be found at the web site located at: **http://www.ridleyengineering.com**

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